What is claimed:

1. A routing system for interconnecting two surface mounted printed circuit boards comprising:

a mid-plane printed circuit board including a first face and a second face, said second face parallel to said first face;

a first printed circuit board surface mounted on said first face of said mid-plane printed circuit board, said first printed circuit board containing pairs of electrical connections;

a second printed circuit board surface mounted on said second face of said mid-plane printed circuit board, said second printed circuit board containing pairs of electrical connections, said second printed circuit boards mounted at an angle to said first printed circuit boards;

a plurality of pairs of via holes on said first and second faces of said mid-plane printed circuit board positioned with respect to the angle of misalignment of said first and second printed circuit boards, said pairs of via holes on said first face of said mid-plane printed circuit board directly overlaying said pairs of via holes on said second face of said mid-plane printed circuit board; and

an plurality of electrical paths through said overlaying pairs of via holes connecting said pairs of electrical connections on said first printed circuit board to said electrical connections on said second printed circuit board.

2. A system as in claim 1, wherein said pairs of via holes are positioned such that:

A. each via hole in each of said pairs of via holes is fixed on an axis perpendicular to an axis that bisects the angle of misalignment of said first and second printed circuit boards; and

B. both via holes in each of said pairs of via holes are equidistant from a point on an axis that bisects the angle of misalignment of said first and second printed circuit boards.

3. A system as in claim 1, wherein said pairs of via holes are positioned such that:

A. each via hole in each of said pairs of via holes is fixed on an axis that bisects the angle of misalignment of said first and second printed circuit boards; and

B. The distance between the first via hole in each of said pairs of via holes and the first electrical connection in one of said pairs of electrical connections is equal to the distance between the second via hole in each of said pairs of via holes and the second electrical connection in one of said pairs of electrical connections.

4. A system as in claim 1, wherein said electrical paths are substantially equal in length.

5. A system as in claim 1, wherein said electrical paths consist of:

a first face electrically conductive surface mount pad mounted on said first face of said mid-plane printed circuit board connecting one of said electrical connections on said first printed circuit board to one of said via holes on said first face of said mid-plane printed circuit board;

an electrically conductive trace connecting each of said via holes on said second face of said mid-plane printed circuit board with the directly overlaying via hole on said first face of said mid-plane printed circuit board; and

a second face electrically conductive surface mount pads mounted on said second face of said mid-plane printed circuit board connecting one of said electrical connections on said second printed circuit board to one of said via holes on said second face of said mid-plane printed circuit board.

6. A system as in claim 5, wherein said electrically conductive traces pass straight through said mid-plane printed circuit board at an angle perpendicular to said mid-plane printed circuit board.

7. A system as in claim 5, wherein said electrically conductive traces are substantially equal in length.

8. A system as in claim 5, wherein said first face electrically conductive surface mount pads are substantially equal in length.

9. A system as in claim 5, wherein said second face electrically conductive surface mount pads are substantially equal in length.

10. A system as in claim 5, wherein said first face electrically conductive surface mount pads are substantially equal in length to said second face electrically conductive surface mount pads.

11. A system as in claim 5, wherein each of said first face surface mount pads connecting the first electrical connection in each of said pairs of electrical connections is a long surface mount pad and each of said first face surface mount pads connecting the second electrical connection in each of said pairs of electrical connections is a short surface mount pad.

12. A system as in claim 11, wherein each of said long surface mount pads is substantially equal in length.

13. A system as in claim 11, wherein each of said short surface mount pads is substantially equal in length.

14. A system as in claim 5, wherein each of said second face surface mount pads connecting the first electrical connection in each of said pairs of electrical connections is a short surface mount pad and each of said second face surface mount pads connecting the second electrical connection in each of said pairs of electrical connections is a long surface mount pad.

15. A system as in claim 14, wherein each of said long surface mount pads is substantially equal in length.

16. A system as in claim 14, wherein each of said short surface mount pads is substantially equal in length.

17. A system as in claim 1, wherein said first and second printed circuit boards are orthogonal.

18. A system as in claim 1, wherein said first and second printed circuit boards are five by eight headers.

19. A system for interconnecting two surface mounted printed circuit boards comprising:

a mid-plane printed circuit board including a first face and a second face, said second face parallel to said first face;

a first printed circuit board surface mounted on said first face of said mid-plane printed circuit board, said first printed circuit board containing pairs of electrical connections;

a second printed circuit board surface mounted on said second face of said mid-plane printed circuit board, said second printed circuit board containing pairs of electrical connections, said second printed circuit boards mounted at an angle to said first printed circuit boards;

a plurality of pairs of via holes on said first and second faces of said mid-plane printed circuit board positioned such that:

A. Each via hole in each of said pairs of via holes is fixed on an axis perpendicular to an axis that bisects the angle of misalignment of said first and second printed circuit boards;

B. Both via holes in each of said pairs of via holes is equidistant from a point on an axis that bisects the angle of misalignment of said first and second printed circuit boards; and

C. Each of said pairs of via holes on said first face of said mid-plane printed circuit board is directly overlaying one of said pairs of via holes on said second face of said mid-plane printed circuit board;

a plurality of electrically conductive traces connecting each of said via holes in said pairs of via hole on said second face of said mid-plane printed circuit board one of said directly overlaying via holes in said pairs of via holes on said first face of said mid-plane printed circuit board, said electrically conductive traces being substantially equal in length;

a plurality of long first face electrically conductive surface mount pads mounted on said first face of said mid-plane printed circuit board, said long first face electrically conductive surface mount pads connecting the first connection in each of said pairs of electrical connections on said first printed circuit board to the first via hole in each of said pairs via holes on said first face of said mid-plane printed circuit board, said long first face electrically conductive surface mount pads being substantially equal in length;

a plurality of short first face electrically conductive surface mount pads mounted on said first face of said mid-plane printed circuit board, said short first face electrically conductive surface mount pads connecting the second connection in each of said pairs of electrical connections on said first printed circuit board to the second via hole in each of said pairs via holes on said first face of said mid-plane printed circuit board, said short first face electrically conductive surface mount pads being substantially equal in length;

a plurality of short second face electrically conductive surface mount pads mounted on said second face of said mid-plane printed circuit board, said short second face electrically conductive surface mount pads connecting the first connection in each of said pairs of electrical connections on said second printed circuit board to the first via hole in each of said pairs via holes on said second face of said mid-plane

printed circuit board, said short second face electrically conductive surface mount pads being substantially equal in length; and

a plurality of long second face electrically conductive surface mount pads mounted on said second face of said mid-plane printed circuit board, each of said long second face electrically conductive surface mount pads connecting the second connection in each of said pairs of electrical connections on said second printed circuit board to the second via hole in each of said pairs via holes on said second face of said mid-plane printed circuit board, said long second face electrically conductive surface mount pads being substantially equal in length.

20. A system for interconnecting two surface mounted printed circuit boards comprising:

a mid-plane printed circuit board including a first face and a second face, said second face parallel to said first face;

a first printed circuit board surface mounted on said first face of said mid-plane printed circuit board, said first printed circuit board containing pairs of electrical connections;

a second printed circuit board surface mounted on said second face of said mid-plane printed circuit board, said second printed circuit board containing pairs of electrical connections, said second printed circuit boards mounted at an angle to said first printed circuit boards;

a plurality of pairs of via holes on said first and second faces of said mid-plane printed circuit board positioned such that:

A. each via hole in each of said second face pairs of via holes is fixed on an axis that bisects the angle of misalignment of said first and second printed circuit boards;

B. The distance between the first via hole in each of said second face pairs of via holes and the first electrical connection in one of said pairs of electrical connections on said second printed circuit board is equal to the distance between the second via hole in each of said second face pairs of via holes and the

second electrical connection in one of said pairs of electrical connections on said second printed circuit board; and

C. each of said pairs of via holes on said first face of said mid-plane printed circuit board is directly overlaying one of said pairs of via holes on said second face of said mid-plane printed circuit board;

a plurality of electrically conductive traces connecting each of said via holes in said pairs of via hole on said second face of said mid-plane printed circuit board one of said directly overlaying via holes in said pairs of via holes on said first face of said mid-plane printed circuit board, said electrically conductive traces being substantially equal in length;

a plurality of first face electrically conductive surface mount pads mounted on said first face of said mid-plane printed circuit board, each of said first face electrically conductive surface mount pads connecting one of said electrical connections on said first printed circuit board to one of said via holes on said first face of said mid-plane printed circuit board, said first face electrically conductive traces being substantially equal in length; and

a plurality of second face electrically conductive surface mount pads mounted on said second face of said mid-plane printed circuit board, each of said second face electrically conductive surface mount pads connecting one of said electrical connections on said second printed circuit board to one of said via holes on said second face of said mid-plane printed circuit board, said second face electrically conductive traces being substantially equal in length to said first face electrically conductive traces.